REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-12 are pending in the application. The Examiner additionally stated that claims 1-12 are rejected. By this amendment, claims 9-10 have been cancelled and claims 1, 2, 4, 5, 6, 7, 8, 11 and 12 have been amended. Hence, claims 1-9, and 11-12 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the File Wrapper

The Examiner notes that the information disclosure statement filed 8/7/01 fails to comply with 37 CFR 1.98(a)(2). Applicant notes that two of these documents are actually part of the continuity data for the present application. The present application is a Continuation-in-part of Serial No. 09/737,375, which claimed priority from Serial No. 60/181,364. The third reference was actually originally submitted under the Disclosure Document program and given DD#492430. A copy of this Document is attached hereto.

In the present Office Action, the Examiner initialed and included PTO Forms 1449 that were previously filed in the present application on 4/7/04. However, another IDS was filed with the PTO on 4/13/04. This IDS was not initialed and proved by the examiner. Applicant has reviewed the Image File Wrapper at the PTO and determined that it was never made part of the file wrapper for this case. However, the IDS was properly submitted via facsimile. Applicant is including herewith a copy of the originally submitted IDS (on 4/13/04), along with the AutoReply confirmation indicating receipt by the PTO. Applicant would appreciate the Examiner considering this art, as originally submitted.

In the Claims

Rejections Under 35 U.S.C. §102(b)

The Examiner rejected claims 1-12 under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent No. 5,559,970 to Sharma (hereinafter Sharma). More specifically, the

Examiner noted that Sharma disclosed a packet processor as claimed. Applicant respectfully traverses the Examiner's rejections.

Before discussing the examiner's rejections, a brief overview of Sharma vis-à-vis Applicant's invention is considered helpful.

Sharma discloses a crossbar switch which interconnects a plurality of processors to a plurality of memory modules. Figure's 1 and 2 of Sharma show multiple processors coupled to his "Self-Routing Crossbar Switch", which in turn is coupled to multiple memory modules. Figure 6 shows buffering mechanisms which store writes from multiple processors to each memory module. That is, if multiple writes are requested, they are serialized and sent to the memory module one by one. Col. 3, lines 55-60.

In contrast, Applicant's invention is not simply serializing packet requests from each processor. Rather, Applicant's invention has to deal with the unique situation in packet processing where a first controller is typically granted priority for read requests. However, a second controller may have read a packet, processed it, and then modified it. The modification MUST be written back into the LPM before it can be read and downloaded by the first controller. This is true whether the write occurs before OR after a read from the first controller is presented, even though the first controller has priority. Applicants have thus provided a novel solution which tracks, for memory cells, writes from the second controller, and performs conflict resolution for the memory cells when the first controller performs a read. Nothing in Sharma is addressed at this novel feature. More specifically, all of the pending requests to a memory, in Sharma, get processed, in the order in which they are serialized (buffered). Nothing in Sharma teaches negating an earlier read request to allow a later write request to complete. Further, nothing in Sharma tracks whether read or write requests are directed at the same cell (or cache line) in memory, nor are the packets in Sharma tagged to allow such comparison.

With respect to claim 1, it is repeated below, as amended, for ease of reference:

1. (Currently amended) In a packet processor having a local packet memory (LPM) for storing packet data during processing, the LPM having a plurality of memory cells, the memory cells accessible by at least one memory access port, a system for managing port contention between at least two controllers that access the memory cells, comprising:

a buffer for queuing write requests to the at least one memory port for a first one of the controllers; and

a logic mechanism associated with the buffer for determining whether a write request from said first one of the controllers is within said buffer and is directed at a first one of the memory cells, and if so, whether a read request exists from a second one of the controllers and is directed at said first one of the memory cells;

wherein, if a read request exists from said second one of the controllers and is directed at said first one of the memory cells while said write request is buffered, said read request is delayed until said write request has completed, regardless of when said read request occurs.

Claim 1, as amended, specifically requires a conflict to exist between a write from a first controller and a read from a second controller, wherein the read is delayed until the write completes. All of this is within the context of packet processing, utilizing a buffer and a logic mechanism for tracking reads/writes to memory cells via a memory access port. As indicated above, nothing in Sharma is directed at delaying a read request from a first controller until a write request from another controller completes. Nor is there anything in Sharma that delays a read request from completing, even though it has a higher priority than the write request, or occurs earlier in time. For these reasons, and those stated above, applicant respectfully requests the examiner to withdraw his rejection of this claim.

Claims 2-6 depend from claim 1 and add further limitations which are neither anticipated nor obviated by Sharma. For the reasons stated above, applicant respectfully requests the examiner to withdraw his rejection of these claims.

With respect to claim 7, it has been amended to substantially comport to be a method counterpart to claim 1 as amended. For all of the reasons stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 8, 11-12, these depend from claim 7 and add further limitations which are neither anticipated nor obviated by Sharma. For the reasons stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of these claims.